| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| S7 | 1 | ("6754099").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2005/05/31 14:21 |
| S9 | 181 | S8 and @pd>"20041228" | US-PGPUB; USPAT; USOCR | OR | OFF | 2005/06/01 09:20 |
| S8 | 1388 | ((257/422) or (365/158)).CCLS. | US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | OFF | 2005/06/01 09:20 |
| S5 | 1170 | ((257/422) or (365/158)).CCLS. | US-PGPUB; USPAT; USOCR | OR | OFF | 2005/06/01 09:20 |
| S2 | 10 | (("5398030") or ("5768181") or ("5946228") or ("6072718") or ("6104633") or ("6242770") or ("6269040") or ("6385082") or ("6388917") or ("6404674")).PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2005/06/01 09:32 |
| S10 | 1 | "6791856" | US-PGPUB; USPAT; USOCR | OR | OFF | 2005/06/01 09:33 |
| S11 | 16 | ("5496759" \| "5748519" \| "5841611" \| "5861328" \| "5892708" \| "5917749" \| "6005798" \| "6005800" \| "6104633" \| "6111782" \| "6134139" \| "6236590" \| "6368878" \| "6424561" \| "6424564" \| "6522574").PN. | US-PGPUB; USPAT; USOCR | OR | OFF | 2005/06/01 10:00 |
| S13 | 132 | (magnetic adj tunnel adj junction) same mram same reference | US-PGPUB; USPAT; USOCR | OR | OFF | 2005/06/01 10:01 |
| S14 | 131 | (magnetic adj tunnel adj junction) and mram and (reference adj cell) | US-PGPUB; USPAT; USOCR | OR | OFF | 2005/06/01 10:02 |
| S12 | 1083 | (magnetic adj tunnel adj junction) and mram and reference | US-PGPUB; USPAT; USOCR | OR | OFF | 2005/06/01 10:02 |

**Search: magnetic tunnel junction AND mram**

**Search: magnetic tunnel junction AND mram AND reference**

# Display from INSPEC

**ANSWER 5**

**Title**

Fully integrated 64 Kb **MRAM** with novel **reference** cell scheme.

**Author**

Jeong, H.S.; Jeong, G.T.; Koh, G.H. (Adv. Technol. Dev., Samsung Electron. Co. Ltd., Kyunggi-Do, South Korea); Song, I.H.; Park, W.J.; Kim, T.W.; Jeong, S.J.; Hwang, Y.N.; Ahn, S.J.; Kim, H.J.; Hong, J.S.; Jeong, W.C.; Lee, S.H.; Park, J.H.; Cho, W.Y.; Kim, J.S.; Song, S.H.; Kim, H.J.; Park, S.O.; Jeong, U.I.; Kim, K.

**Publication Source**

International Electron Devices Meeting. Technical Digest (Cat. No.02CH37358)
Piscataway, NJ, USA: IEEE, 2002. p.551-4 of 957 pp. 4 refs.
Conference: San Francisco, CA, USA, 8-11 Dec 2002
Sponsor(s): Electron. Devices Soc. IEEE
Price: CCCC 0-7803-7462-2/02/$17.00
ISBN: 0-7803-7462-2

**Document Type**

Conference Article

**Treatment Code**

New Development; Practical; Experimental

**Country of Publication**

United States

**Language**

English

**Abstract**

We have fully integrated a 64 Kb **MRAM** with 0.24 mu m-CMOS technology. A new sensing scheme employing a separated half-current source is adopted for the **reference** bit line to increase the sensing signal. To reduce cell resistance, a Co salicidation process is applied to transistor formation. In key fabrication processes, the roughness of the buffer layer, on which the MTJs are stacked, is reduced by using Ru on the TiN bottom electrode, and magnetic disturbance is avoided by depositing TiN hard masks on the MTJ under low-power and low-temperature conditions. The tunneling barrier micro-bridge due to the attachment of

by-products during etching is completely eliminated by adopting a 2-step MTJ etch with an introduced capping oxide layer. Consequently, MR values of >30% are found in more than 90% of chips.

**Classification Code**

B1265D Memory circuits; B2570D CMOS integrated circuits; B3120J Magneto-acoustic, magnetoresistive, magnetostrictive and magnetostatic wave devices; B2550F Metallisation and interconnection technology; B2550E Surface treatment (semiconductor technology)

**Controlled Indexing**

CMOS MEMORY CIRCUITS; INTEGRATED CIRCUIT METALLISATION; MAGNETIC STORAGE; MAGNETIC TUNNELLING; MAGNETOELECTRONICS; RANDOM-ACCESS STORAGE; SPUTTER ETCHING; SURFACE TOPOGRAPHY

**Element Terms**

Co; Ru; N*Ti; TiN; Ti cp; cp; N cp; Co*Si; Co sy 2; sy 2; Si sy 2; CoSi2; Co cp; Si cp; N*Ru*Ti; N sy 3; sy 3; Ru sy 3; Ti sy 3; Ru-TiN; CoSi; Si; Ti

**Supplementary Indexing**

**CMOS fully integrated 64 Kb MRAM**; **reference cell scheme**; **magnetic tunnel junctions**; 0.24 mu m-CMOS technology; sensing scheme; separated half-current source; **reference bit line**; cell resistance; Co salicidation process; transistor formation; buffer layer roughness; TiN bottom electrode; magnetic disturbance avoidance; TiN hard mask; low-power low-temperature conditions; tunneling barrier micro-bridge elimination; two-step etch; capping oxide layer; 64 Kbit; 0.24 micron; CoSi2; Ru-TiN

**Chemical Indexing**

CoSi2 int, Si2 int, Co int, Si int, CoSi2 bin, Si2 bin, Co bin, Si bin; Ru-TiN int, TiN int, Ru int, Ti int, N int, TiN bin, Ti bin, N bin, Ru el

**Physical Properties**

storage capacity 6.6E+04 bit; size 2.4E-07 m

**Accession Number**

2003:7509347 INSPEC

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**ANSWER 6**

**Title**

Developments in RAMs (random access memories): FeRAMs and **MRAMs**: part 2.

**Author**

Sikora, A.

**Publication Source**

Elektronik (19 March 2002) vol.51, no.6, p.52-7. 16 refs.
Published by: WEKA-Fachzeitschriften
CODEN: EKRKAR ISSN: 0013-5658
SICI: 0013-5658(20020319)51:6L.52:DRRA;1-H

**Document Type**

Journal

**Treatment Code**

Application; General Review; Practical

**Country of Publication**

Germany, Federal Republic of

**Language**

German

**Abstract**

For pt. see ibid., no. 5, p. 66 (2002). Discusses **magnetic** RAMs, Ovonics Unified Memory and polymer-based ferroelectric random access memories. Illustrates the original Rajchman ferromagnetic ring core memory, and presents a diagram of a hybrid **MRAM** cell. Also shows a "**magnetic tunnel junction**" (MTJ) memory, which operates by filtering electron spin polarisation, and explains its operation. A giant magnetorestive effect (GMR) memory cell is shown, which employs ferromagnetic film layers separated by conducting layers. **Reference** is made to pseudo-spin valve (PSV) technology, also based on the magneto-resistive effect. Examines commercial prospects for **magnetic tunnel junction** memories. Diagrams of a molecular ferro-electric polymer RAM and a polymer-based FeRAM memory (polymers between metal tracks) are presented.

**Classification Code**

B1265D Memory circuits; B2860F Ferroelectric devices; B3120N Magnetic thin film devices; B3120J Magneto-acoustic, magnetoresistive, magnetostrictive and magnetostatic wave devices

**Controlled Indexing**

FERROELECTRIC STORAGE; MAGNETIC FILM STORES; MAGNETORESISTIVE DEVICES; RANDOM-ACCESS STORAGE

**Supplementary Indexing**

RAMs; FeRAMs; **MRAMs**; magnetic RAMs; Ovonics Unified Memory; polymer-based ferro-electric memories; Rajchman ferromagnetic ring core memory; hybrid cell; **magnetic tunnel junction**; electron spin polarisation; GMR; ferromagnetic film layers; conducting layers; pseudo-spin valve technology; magneto-resistive effect

**Accession Number**

2002:7263848 INSPEC

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# Display from PASCAL



**Title in English**

A High-Speed 128-kb **MRAM** Core for Future Universal Memory Applications

**Author**

DEBROSSE J.; GOGL D.; BETTE A.; HOENIGSCHMID H.; ROBERTAZZI R.; ARNDT C.; BRAUN D.; CASAROTTO D.; HAVRELUK R.; LAMMERS S.; OBERMAIER W.; REOHR W. R.; VIEHMANN H.; GALLAGHER W. J.; MULLER G.

**Organization**

IBM Microelectronics, Essex Junction, VT 05452, United States

**Publication Source**

IEEE Journal of Solid-State Circuits, (2004), 39(4), 678-683, 4 refs.
ISSN: 0018-9200 CODEN: IJSCBC

**Document Type**

Journal

**Bibliographic Level**

Analytic

**Country of Publication**

United States

**Language**

English

**Abstract**

A 128-kb **magnetic** random access memory (**MRAM**) test chip has been fabricated utilizing, for the first time, a 0.18-.mu.m VDD = 1-8 V logic process technology with Cu metallization. The presented design uses a 1.4-.mu.m2 one-transistor/one-**magnetic tunnel junction** (1T1MTJ) cell and features a symmetrical high-speed sensing architecture using complementary **reference** cells and configurable load devices. Extrapolations from test chip measurements and circuit assessments predict a 5-ns random array read access time and random write operations with <5-ns write pulse width.

**Availability**

INIST-222 L

**Accession Number**

2004-0198708 PASCAL

**Classification Code**

001D03I02; Applied sciences; Electronics; Information storage, Information reproduction
001D03F; Applied sciences; Electronics; Microelectronics, Solid state devices
001B30; Physics; Atomic physics, Molecular physics
001D05I01; Applied sciences; Electrical engineering; Electrical power engineering
001D05A; Applied sciences; Electrical engineering
001D11C06D; Applied sciences; Metals, Metallurgy, Materials science; Metallic material transformation
240; Metals, Metallurgy, Materials science

**Classification Code (French)**

001D03I02; Sciences appliquees; Electronique; Stockage de l'information, Lecture de l'information
001D03F; Sciences appliquees; Electronique; Microelectronique, Dispositifs a l'etat solide
001B30; Physique; Physique atomique, Physique moleculaire
001D05I01; Sciences appliquees; Electrotechnique; Electroenergetique
001D05A; Sciences appliquees; Electrotechnique
001D11C06D; Sciences appliquees; Metaux, Metallurgie, Science des materiaux; Transformation de materiaux metalliques
240; Metaux, Metallurgie, Science des materiaux

**Classification Code (Spanish)**

001D03I02; Ciencias aplicadas; Electronica; Almaceniamento de la informacion, Lectura de la informacion
001D03F; Ciencias aplicadas; Electronica; Microelectronica, Dispositivos en el estado solido
001B30; Fisica; Fisica atomica, Fisica molecular
001D05I01; Ciencias aplicadas; Electrotecnica; Electroenergetica

001D05A; Ciencias aplicadas; Electrotecnica
001D11C06D; Ciencias aplicadas; Metales, Metalurgia, Ciencia de los materiales; Transformacion de materiales metalicos
240; Metales, Metalurgia, Ciencia de los materiales

**Controlled Indexing**

Access time; **Reference** cells; Universal memory; Application; Microprocessor chips; Electron tunneling; Electric loads; Electric resistance; Electric potential; Metallizing; Logic design; Extrapolation; Random access storage; Theory

**Controlled Term (in French)**

Application; Puce microprocesseur; Effet tunnel electronique; Charge reseau electrique; Resistance electrique; Potentiel electrique; Metallisation; Conception logique; Extrapolation; Memoire acces direct; Theorie

**Controlled Term in German**

Anwendung

**Controlled Term (in Spanish)**

Aplicacion

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**Session Cost: $11.71**

Wed, 1 Jun 2005, 9:51:55 AM EST

Edit an existing query or compose a new query in the Search Query Display.

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- Combine search queries using AND, OR, or NOT
- Delete a search
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| | |
|---|---|
| #1 | ( mram<in>metadata ) <and> ( magnetic tunnel junction<in>metadata ) |
| #2 | ( mram<in>metadata ) <and> ( magnetic tunnel junction<in>metadata ) |
| #3 | ( mram<in>metadata ) <and> ( magnetic tunnel junction<in>metadata ) |
| #4 | ( mram<in>metadata ) <and> ( magnetic tunnel junction<in>metadata ) |
| #5 | ( mram<in>metadata ) <and> ( magnetic tunnel junction<in>metadata ) |
| #6 | ( mram<in>metadata ) <and> ( magnetic tunnel junction<in>metadata ) <and> (reference<in>metadata) |
| #7 | ( mram<in>metadata ) <and> ( magnetic tunnel junction<in>metadata ) <and> (reference<in>metadata) |

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